Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for fabricating a semiconductor device having a gate structure on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the method comprising the steps of :
removing material in a gate region of the device to expose a portion of the substrate;
forming a gate dielectric on the exposed portion of the substrate;
forming a metal layer overlying the gate dielectric and the dielectric material;
forming a silicon layer overlying the metal layer;
removing a first portion of the metal layer and a first portion of the silicon layer, so that the top surface of the dielectric material is exposed and a second portion of the metal layer and a second portion of the silicon layer remain in the gate region and have surfaces coplanar with said top surface; and
forming a silicide contact in the gate region, in contact with the second portion of the metal layer.

[c2] A method according to claim 1, wherein said step of forming a silicide contact further comprises:

depositing a layer of a silicide-forming metal over the gate region;
performing a siliciding process to form a metal silicide including silicon from the second portion of the silicon layer and metal from said layer of silicide-forming metal; and
performing a planarization process to expose the top surface of the dielectric material.

[c3] A method according to claim 1, wherein the silicide-forming metal is selected from the group consisting of Ni, Co, Ta, W and Mo.

[c4] A method according to claim 1, wherein
said step of removing material in the gate region forms a trench having sidewalls and a bottom, the bottom being the exposed portion of the substrate,
said step of forming the metal layer further comprises forming metal on the sidewalls of the trench, and
said step of forming the silicon layer comprises filling the trench.

[c5] A method according to claim 1, wherein the semiconductor device is fabricated on a wafer, said step of forming the metal layer comprises forming a blanket metal layer on the wafer, and said step of forming the silicon layer comprises forming a blanket silicon layer on the

wafer.

[c6] A method for fabricating a semiconductor device having a gate structure on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the method comprising the steps of :
removing material in a first portion of a gate region of the device to expose a first portion of the substrate;
forming a first gate dielectric on the exposed first portion of the substrate;
forming a first metal layer overlying the first gate dielectric;
forming a first silicon layer overlying the first metal layer;
removing a first portion of the first metal layer and a first portion of the first silicon layer, so that the top surface of the dielectric material is exposed and a second portion of the first metal layer and a second portion of the first silicon layer remain in the gate region and have surfaces coplanar with said top surface;
removing material in a second portion of the gate region to expose a second portion of the substrate and to expose an adjacent portion of the first metal layer;
forming a second gate dielectric on the exposed second portion of the substrate;
forming an oxide layer on said exposed adjacent portion

of the first metal layer;
forming a second metal layer overlying the second gate dielectric;
forming a second silicon layer overlying second metal layer;
removing a first portion of the second metal layer and a first portion of the second silicon layer, so that the top surface of the dielectric material is exposed and a second portion of the second metal layer and a second portion of the second silicon layer remain in the gate region and have surfaces coplanar with said top surface; and
forming a silicide contact in the gate region, in contact with the second portion of the first metal layer and the second portion of the second metal layer.

[c7] A method according to claim 6, wherein said step of forming a silicide contact further comprises:
forming a third silicon layer overlying the first portion of the gate region and the second portion of the gate region;
depositing a layer of a silicide-forming metal over the third silicon layer;
performing a siliciding process to form a metal silicide including silicon from the second portion of the first silicon layer, from the second portion of the second silicon layer and from the third silicon layer, and metal from

said layer of silicide-forming metal; and
performing a planarization process to expose the top surface of the dielectric material.

[c8] A method according to claim 6, wherein the silicide-forming metal is selected from the group consisting of Ni, Co, Ta, W and Mo.

[c9] A method according to claim 6, wherein
said step of removing material in the first portion of the gate region forms a first trench having sidewalls and a bottom, the bottom being the exposed first portion of the substrate,
said step of forming the first metal layer further comprises forming metal on the sidewalls of the first trench,
said step of forming the first silicon layer comprises filling the first trench,
said step of removing material in the second portion of the gate region forms a second trench having sidewalls and a bottom, the bottom being the exposed second portion of the substrate,
said step of forming the second metal layer further comprises forming metal on the sidewalls of the second trench, and
said step of forming the second silicon layer comprises filling the second trench.

[c10] A method according to claim 6, wherein the semiconductor device is fabricated on a wafer, said step of forming the first metal layer comprises forming a first blanket metal layer on the wafer, said step of forming the first silicon layer comprises forming a second blanket silicon layer on the wafer, said step of forming the second metal layer comprises forming a second blanket metal layer on the wafer, and said step of forming the second silicon layer comprises forming a second blanket silicon layer on the wafer.

[c11] A method according to claim 6, further comprising the step of:
prior to said step of forming a silicide contact, removing metal and metal oxide so that the second portion of the first metal layer, the oxide layer and the second portion of the second metal layer are recessed with respect to said top surface.

[c12] A method according to claim 7, further comprising the step of:
prior to said step of forming a silicide contact, removing metal and metal oxide so that the second portion of the first metal layer, the oxide layer and the second portion of the second metal layer are recessed with respect to said top surface, thereby forming a recess in the gate region; and wherein said step of forming the third silicon

layer further comprises filling the recess.

[c13] A method according to claim 12, wherein said step of forming the silicide contact causes the silicide to fill the recess.

[c14] A method according to claim 6, further comprising the step offorming a nitride layer overlying the gate region, after said step of forming the silicide contact.

[c15] A method according to claim 6, where said silicide contact is recessed with respect to said top surface, thereby forming a recess in the gate region, and further comprising the steps of:
forming a nitride layer overlying the gate region and filling said recess; and
performing a planarization process to expose said top surface, so that a portion of the nitride layer remains in said recess and has a surface coplanar with said top surface.

[c16] A semiconductor device having a gate structure on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the device comprising:
a gate dielectric overlying a portion of the substrate in a gate region and in contact therewith;
a metal layer in contact with the gate dielectric; and

a silicide contact having a lower surface in contact with the metal layer and an upper surface coplanar with said top surface.

[c17] A semiconductor device according to claim 16, wherein the gate region is characterized as a trench having a bottom and sidewalls, the gate dielectric overlies the bottom of the trench, the metal layer is in contact with the sidewalls of the trench, and the silicide contact fills the trench.

[c18] A semiconductor device according to claim 16, wherein the metal layer comprises a first metal layer and a second metal layer, and further comprises a metal oxide layer between the first metal layer and the second metal layer.

[c19] A semiconductor device according to claim 16, further comprising a nitride layer overlying the silicide contact.

[c20] A semiconductor device according to claim 16, wherein the silicide contact comprises:
a silicide portion having an upper surface recessed with the respect to said top surface; and
a nitride cap portion overlying the silicide portion and having an upper surface coplanar with said top surface, the nitride cap portion being self-aligned to the gate re-

gion.